FAQ Guide

PXNplus and M3000 enclosure

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Compatibility

Q: What version of Picture Perfect will support the PXNplus CPU?

A: Picture Perfect 2.0 or higher supports the PXNplus CPU. The PXNplus can be installed in a M5, M2000 or and M3000 enclosure.

Q: What version of Secure Perfect will support the PXNplus CPU?

A: Secure Perfect 6.1.1 or higher supports the PXNplus CPU. The PXNplus can be installed in a M5, M2000 or and M3000 enclosure. Secure Perfect 6.1.1 has been shipping since July 2005.

Q: Can a PX/PXN CPU be in the same communications chain (either upstream or downstream) as a PXNplus?

A: Yes. The PXNplus can co-exist in a mix line of PX and PXN microcontrollers. There are no restrictions against these configurations. A PXNplus can be the head of line microcontroller for 7 downstream PXs or you can have up to seven downstream PXNplus microcontrollers downstream from a PX or PXN microcontroller. Overall a recommendation to limit communications lines to 64 readers still remains regardless to CPU type.

Q: Are there any limitations FLASHing a mixed line of CPUs?

A: No. The host for the PXNplus or the PX/PXN CPU will download the correct file into the controller. The hex files (EFL) Flashed to a PXNplus are different than the hex files for a PX or PXN microcontroller. The CPUs will not allow an incorrect EFL file type to be loaded.

Q: How do I launch the web pages from a PXNplus that is downstream of either a PX/PXN/PXNplus?

A: You would have to attach via Ethernet locally to the downstream PXNplus. Generally this means that someone would have to take a laptop to the field and use a crossover cable to connect to the downstream PXNplus controller. The downstream PXNplus controller can be directly FLASHed from its host (either Picture Perfect or Secure Perfect). But changes to the PXNplus communications configuration and viewing log files can only be done through the on-board browser-based integrated configuration tool via Ethernet.

This is one of the main reasons why GE Security recommends that installations not consider using downstream serial microcontrollers. The ability to directly communicate with serial devices is much less than with network attached devices.

Q: Are there any limitations installing PXNplus CPUs in older microcontroller enclosures?

A: The minimum board revision levels supported by the PXNplus CPU are:

Option Board	Part Number	Current Release	PXplus min rev level	Rev Date
2 RP	110063001	N	E	4/15/1998
20 DI	110072001	D	B	9/2/1997
8 RP	110100001	J	G	6/23/1998
2 SRP	110101001	D	A (any)	N/A
16 DOR	110078001	D	A (any)	N/A
16 DO	110071001	G	D	7/6/1999
Pwr/Comm	110064001	M	J	9/22/1999
Backplane	110061001	C	A (any)	N/A

Q: What reader, input and output boards does the PXNplus support?

A: Interface Boards supported by the PXNplus CPU: 2RP, S2RP, 8RP, CK8RP, 20 DI, 16 DO, 16 DOR, Power / Comm, and the 2000 Interface board.

Q: Can the PXNplus CPU work with M/2 or M/4 controllers?

A: The M/2 and M/4 controllers have not been tested with the PXNplus CPU card. GE Security does not recommend the usage of M/2 or M/4 with PXNplus.

Trade-In Program

Q: Will this program expire?

A: GE Security must receive Purchase Orders for the PXNplus CPU board packages prior to 7/31/2006 in order to qualify for the Trade-In Program. The integrator must return the old CPU boards under RMA by 12/31/06 in order to qualify for credit.

Q: What are the program highlights?

A: GE Security is offering three convenient packages of PXNplus CPU boards (preconfigured for either Picture Perfect or Secure Perfect). An integrator will purchase their choice of 10, 50 or 100-packs to replace existing in-field CPUs. When the upgrade is complete, the integrator will contact GE Security to receive an RMA for return of replaced PX, PXN, P, or E CPU boards. The integrator will ship the equal quantity of replaced CPU boards back to GE Security, and GE Security will credit the integrator account. The number of boards returned must equal the same number as in the packs originally ordered.

Q: What if I need more PXNplus CPUs than are offered in the packages?

A: An integrator can purchase multiple packs to achieve the necessary quantity of CPU board replacements.

Q: What part numbers do I order to get a 10, 50 or 100 pack of PXNplus CPUs?

A:

Description	Part Number
10 Pack Upgrade PXNplus CPU Boards Picture Perfect	521216001
10 Pack Upgrade PXNplus CPU Boards Secure Perfect	521216002
50 Pack Upgrade PXNplus CPU Boards Picture Perfect	521216003
50 Pack Upgrade PXNplus CPU Boards Secure Perfect	521216004
100 Pack Upgrade PXNplus CPU Boards Picture Perfect	521216005
100 Pack Upgrade PXNplus CPU Boards Secure Perfect	521216006

Upgrade instructions are provided in the pack shipping materials.

Q: How will I receive credit for my returned CPU boards?

A: The number of boards returned must be equal to the number of boards ordered. A credit memo will be issued when the 10, 50 or 100-pack of old CPU boards with proper RMA information are returned to GE Security.

Q: How much credit will I receive for the old CPU boards?

A: Each upgrade pack has a credit value:

Description	Part Number	Credit upon return of old CPUs under RMA
10 Pack Upgrade PXNplus CPU Boards Picture Perfect	521216001	$4,500
10 Pack Upgrade PXNplus CPU Boards Secure Perfect	521216002	$4,500
50 Pack Upgrade PXNplus CPU Boards Picture Perfect	521216003	$27,500
50 Pack Upgrade PXNplus CPU Boards Secure Perfect	521216004	$27,500
100 Pack Upgrade PXNplus CPU Boards Picture Perfect	521216005	$65,000
100 Pack Upgrade PXNplus CPU Boards Secure Perfect	521216006	$65,000

Q: What types of CPU boards can I return?

A: Any CASI M5 or M2000 based CPU is eligible for this trade-in program. This includes the M/5- E CPU, the M/5-P CPU, the M/5-PX CPU and the M/5-PXN CPU. The PX- and PXN-based CPUs in M2000s are also eligible.

Q: How do I request an RMA for this program?

A: Register online at http://www.gesecurity.com/pxnplusrebate or contact your GE District Manager for a PXNplus Rebate Application Form to fax to (561) 998-6160.

M3000 Enclosure

Q: What are the dimensions of the enclosure?

A: 17 inches (431mm) x 15.6 inches (396mm) x 6.2 inches (158mm)

Q: What is included when I purchase the enclosure?

A: The enclosure is constructed from gavannealed steel, which has a gray powder-coat textured paint. Inside the enclosure there is a C-bracket which holds the controller boards, a passive backplane which the controller boards plug into, a PXNplus CPU board and a Power/Comm board. The passive backplane has five open slots for controller option boards. There is a pre-wired tamper switch attached to the enclosure. There is a 6 Amp power supply mounted on a DIN rail in the enclosure also. The power supply input can range from 90 to 260 VAC and 50/60 Hz. The Power Supply output wiring is pre-wired to the Power/Comm board. A 7 Amp/hr gel-cell battery is included with the enclosure. There is a key lock on the cabinet door.

Q: How long does the battery backup last?

A: Battery life depends on usage. Typically, the 7 Amp/hr battery should be able to last at least 4 hours.

Shorter battery backup time may be experienced if high current draw Proximity readers are used or if there is high reader traffic.

Q: Can I power strikes from the M3000?

A: No, you should not power strikes from the power supply included with the M3000 enclos

ure. There is a separate offering of the same 6 Amp power supply in a smaller enclosure that is intended to be used for either powering a M5 enclosure or for door strikes. Its part number is 300377001.

PXNplus Features

Q: What does DHCP mean for me?

A: Short for Dynamic Host Configuration Protocol, a protocol for assigning dynamic IP addresses to devices on a network. With dynamic addressing, a device can have a different IP address every time it connects to the network. In some systems, the device's IP address can even change while it is still connected.

Dynamic addressing simplifies network administration because the software keeps track of IP addresses rather than requiring an administrator to manage the task. This means that a new computer can be added to a network without the hassle of manually assigning it a unique IP address.

So the PXNplus CPU can use a DHCP assigned address as opposed to a fixed IP number address. This is a very important issue for IT departments when they are re-configuring their network. Fixed IP addresses must be manually adjusted, device by device, while DHCP based controllers can be reconfigured on the fly.

Q: How does the persistent memory in the PXNplus work?

A: Data stored in the PXNplus memory includes badge information, reader, alarm, and output configuration and device schedules. This information is sent from the host to each controller in the system. The PXNplus uses this information to make real-time decisions about whether to grant or deny access, to create an alarm event or trigger an output based on an input going active.

The information the PXNplus receives from its host is stored in FLASH memory. FLASH memory is non-volatile, so the information persists, even after a power loss. If a PXNplus microcontroller experiences a power loss, one of two conditions will confront the microcontroller when power is restored: 1) The PXNplus microcontroller will be able to communicate to its host; or, 2) the PXNplus microcontroller will not be able to communicate to its host. If the first condition exists, then as normal, the controller will request a new database from its host so the controller can synchronize with the host database. The host will automatically send the microcontroller its new database. If the second condition exists, and the microcontroller cannot communicate to its host, then the controller will read its database from its local FLASH memory. The PXNplus CPU will then have its original database and it will know the current date and time from its on-board real-time clock, so it will immediately begin normal operations of granting or deny access and run-

ning schedules. When host communications is restored, the PXNplus will automatically upload historical transactions that it buffered while it could not communicate to the host, and then it will automatically receive a new database from the host, so the PXNplus will be synchronized with any changes that might have occurred at the host.

A super-capacitor is used to continuously power a real-time clock in the PXNplus CPU. The super-capacitor will run the real-time clock without external power for about 30 days.

Q: Can the PXNplus support HID iClass readers and US Government FIPS 201 type IDs?

A: Yes. The HID iClass readers can read the CHUID from a FIPS 201 compliant credential. The iClass readers will then output a FASC-N number to the PXNplus controller in a 64 bit BCD format. The iClass reader can be wired directly to a 2RP or and S2RP reader interface board within the PXNplus microcontroller (in either a M5 or M3000 enclosure). Alternatively, the iClass reader can be wired to a WIU-4- FIPS, that will transform the Wiegand data stream to a Supervised F2F data stream. This will permit the use of either an 8RP in a M5 or M3000 enclosure or 2000 interface board in a M2000 enclosure.

Q: Is the PXNplus UL 294 and 1076 approved?

A: Yes, the PXNplus has passed UL 294 and 1076 testing. Additionally, the PXNplus has CE and FCC approvals.