



GE Interlogix

# Micro/5-PX

## Micro/5-PX CPU Board Overview

The Micro/5-PX CPU board is a switchless micro. This board is used with **Picture Perfect** Version 1.5 or later and **Secure Perfect** Version 2.0 or later. For configuration of this board within **Picture Perfect** software, refer to the *Picture Perfect Administration Guide*.

**NOTE** The Micro/5-PX CPU Board (110124-006) comes with 8MB of RAM.



### Picture Perfect Version 1.5 or Later

- **Direct-Connect Micro:** Board addressing is done by configuring the micro location within the **Picture Perfect** software. When **Picture Perfect** is started, the first micro in the chain of micros talks to the host who responds by giving the micro its address. Then the second micro in the chain talks to the host and receives its address. This process continues until all micros have received their address.
- **Dial-Up Micro:** Use the micro firmware installation tools to set the address and the phone number. See the MICTOOL online help for additional information.
- The number of badges a **Picture Perfect** Micro/5-PX micro can hold varies according to RAM.

Table 1: Picture Perfect RAM Version and Number of Badges

RAM Version	Number of Badges
2M	28,000
4M	84,000
8M	196,000

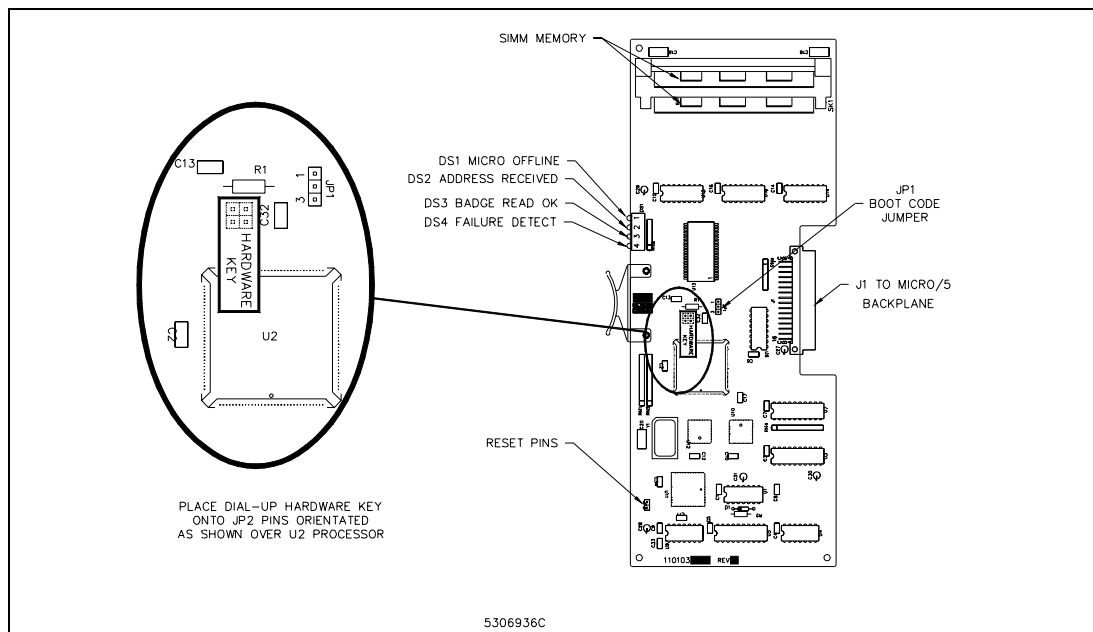
### Secure Perfect Version 2.0 or Later

- **Direct Connect or Dial-Up Micro:** Use micro firmware installation tools to set board address. See the MICTOOL online help for additional information.
- The number of badges and readers a Micro/5-PX micro can hold varies according to the **Secure Perfect** version.

**Table 2: Secure Perfect and RAM Versions and Number of Badges and Readers**

Secure Perfect Version	RAM Version	Number of Badges	Number of Readers
2.0 or earlier	2M	4,000	8
2.1	2M	28,000	16

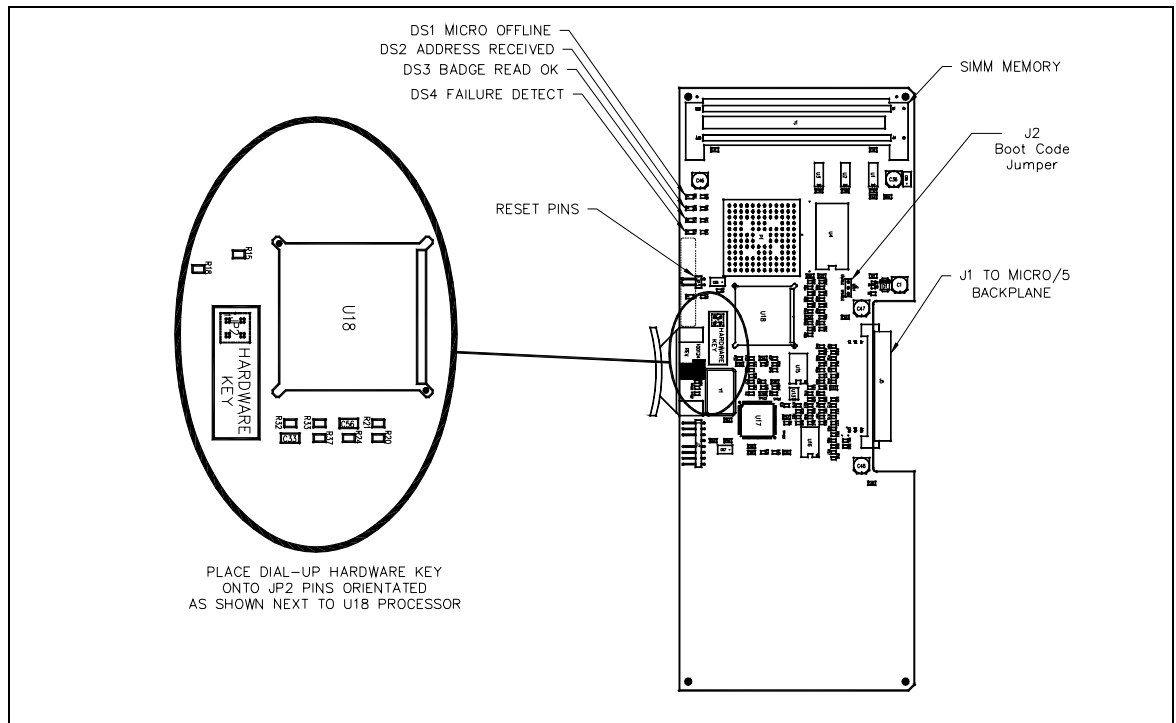
Micro/5-PX board layout is shown in Figures 1, 2, and 3.



**Figure 1: Micro/5-PX CPU Board Layout (110103-00X)**

**NOTE** If using Picture Perfect firmware version 1.5.9 or higher, the hardware key is no longer required.



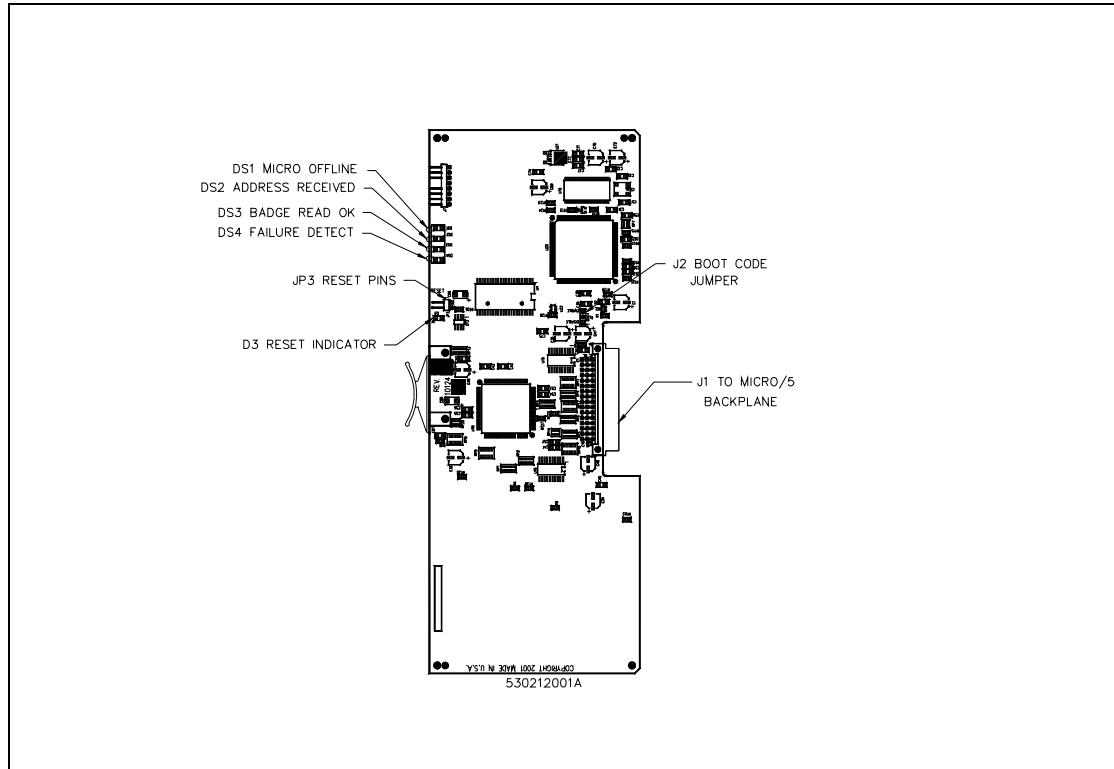


**Figure 2: Micro/5-PX CPU Board Layout (110124-00X)**

**NOTE**

If using Picture Perfect firmware version 1.5.9 or higher, the hardware key is no longer required.





**Figure 3: Micro/5-PX CPU Board Layout (110124-006)**

## LEDs Function

Looking at the LEDs on an installed CPU board, the top LED is DS1.

**Table 3: Micro/5-PX CPU Board LEDs**

LED Number	State in Maintenance Mode	State When Application is Running
DS1	OFF	ON = Micro Offline
DS2	OFF	ON = Address Received
DS3	ON	ON = Badge Read OK
DS4	OFF	ON = CPU Failure Detected Flashing = Waiting for Database

**Maintenance mode:** Micro/5-PX must be in maintenance mode before any application (personality) is downloaded to its flash EEPROM. See the MICTOOL online help for instructions on downloading a personality to EEPROM.

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## DIP Switch Settings

There are no switch settings on Micro/5-PX CPU board.

- **Picture Perfect** systems; addressing is configured within software. When **Picture Perfect** is started, first micro in chain of micros talks to host who responds by giving that micro its address. Then second micro in the chain talks to host and receives its address. This process continues until all micros have received their address.
- **Secure Perfect** systems; micro address must be set with micro firmware installation tools.

## Jumpers

The jumpers as described in Table 4, Boot Code Jumper are for the purposes of:

- **Program Boot.** This is the program boot portion of the flash memory which is factory-programmed and should not be changed
- **Run Application.** These jumpers should be set as described in Table 4, Boot Code Jumper in order for the Micro/5-PX CPU board to be programmed properly.

**Table 4: Boot Code Jumper**

Board	Jumper	Pins	Function
100103 -	JP1	1 and 2	Program Boot
		2 and 3	Run Application
100124 -	J2	2 and 3	Program Boot
		1 and 2	Run Application

## Application Code (Firmware)

To download application code (i.e., firmware) refer to the MICTOOL online help. You will need to download firmware when:

- a micro is in maintenance mode. Refer to Table 3, Micro/5-PX CPU Board LEDs,” on page 4 for LEDs state when micro is in maintenance mode.
- upgrading to a newer version of application code.

If you wish to erase a Micro/5-PX application code, refer to Micro Configuration Utility.

## Micro/2 Downstream Support

If you plan to include Micro/2s downstream from a Micro/5-PX, consider the following items:

- **Secure Perfect** - Version 2.1 or later; can support downstream Micro/2s.

- **Picture Perfect** - Version 1.4.6 or later; supports, using Micro/5-PX firmware, 8 downstream Micro/2s with 64 readers total capacity.
- **Picture Perfect** - If there is no micro defined downstream on **Picture Perfect Micros** form, then default is set for Micro/2s downstream.
- **If Micro/5-PX is configured for Micro/2s downstream** - no Micro/5-P, Micro/5-PX, Micro/5-PXN or Micro/4-P can be downstream.
- **If downstream Micro/2s are same board number as first Micro/5-PX reader board** - first 2 readers per Micro/2 cannot be used. In some situations, this can be remedied (as seen in Example 1). In others, you will lose the first two reader ports (as seen in Example 2). However, this is site-dependent.

#### NOTE



For information on wiring Micro/5s to Micro/2s, refer to wiring microcontrollers in the *Micro/5 Installation Guide*, Chapter 3.

#### Example 1: Problem

Micro/5-PX configured with one 2RP board addressed as Board 1, Readers 0 and 1. Downstream Micro/2 is addressed as Board 1, Readers 0 through 7. There will be a conflict since both micros are using Readers 0 and 1 on Board 1.

**PROBLEM!**

Micro/5-PX (2RP)		Micro/2	
Board	Reader	Board	Reader
1	0	1	0
	1		1
			2
			3
			4
			5
			6
			7

#### Example 1: Solution

Since there are no other micros, downstream Micro/2 can be addressed as Board 2. Now all readers in Micro/2 can be used.

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**OK!**

Micro/5-PX (2RP)		Micro/2	
Board	Reader	Board	Reader
1	0	2	0
	1		1
			2
			3
			4
			5
			6
			7

Sometimes, it's not that easy. See the next example.

### Example 2: Problem

There are two 8RP boards in the Micro/5-PX. The 8RP boards are addressed as Board 1, Readers 0 and 1; Board 2, Readers 0 and 1; and so on. The first downstream Micro/2 is addressed as Board 1, Readers 0 through 7 and the second downstream Micro/2 is addressed as Board 2, Readers 0 through 7. Since both micros are using Readers 0 and 1 on Board 1 and Board 2, a problem will arise.

**PROBLEM!**

Micro/5-PX (2 8RPs)		Micro/2		Micro/2	
Board	Reader	Board	Reader	Board	Reader
1	0	1	0	2	0
	1		1		1
2	0		2		2
	1		3		3
3	0		4		4
	1		5		5
4	0		6		6
	1		7		7
5	0	<b>PROBLEM!</b>			
	1				
6	0				
	1				
7	0				
	1				
8	0				
	1				

### Example 2: Solution

If only Readers 0 through 4 on the Micro/2 are being used, then address those readers as 2 through 6. If all readers are being used, then two of those readers will have to be disabled (not used).

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